Amendments to the Specification:

Please replace paragraph [0028] with the following amended paragraph:

[0028] In describing the operation of the apparatus of FIG. 3, it is assumed that initially, there is no synchronization; i.e., the apparatus 300 does not know where the synchronization bits are within the serial data stream that is being received and is in an out of sync state. The input serial data stream D(i) is shifted bitwise (at a rate of 10 Gb/sec) into a serial-to-parallel (S/P) converter [[304]] 303. The S/P converter 303 is 128 bits long (or wide) and can be implemented using a shift register or the like.

Please replace paragraph [0035] with the following amended paragraph:

[0035] In an exemplary embodiment, the exhausted guess register 318 may comprise a 66-bit register, with each of the states of FIG. 2 having a corresponding bit. The status of a bit in the exhausted guess register 318 indicates whether the corresponding state has been exhausted as a valid guess. Whenever the state guess block 306 generates a guess, the guessed at state is noted in the exhausted guess register [[306]] 318 by setting its corresponding bit. The exhausted guess register 318 is cleared upon entry into the synchronization state (described below) or upon exit therefrom. The exhausted guess register [[306]] 318 is used (i.e., not reset) when the synchronization mechanism is in the slip state (i.e., seeking synchronization). Exiting the synchronization state necessitates execution of the sync acquisition method from scratch. The exhausted guess register may also be cleared when all of its bits are set and synchronization has not been achieved.